

**REMARKS**

Please reconsider the application in view of the above amendments and the following remarks.

**I. Objection to the Specification**

The Examiner objected to the Specification because the Specification contained numbers in brackets at the beginning of every paragraph. In response, Applicant has submitted (herein as part of Appendix A) a substitute Specification in which the bracketed paragraph numbers have been removed. No matter has been amended or added by way of the substitute Specification. Accordingly, Applicant respectfully requests withdrawal of the objection to the Specification.

**II. Objections to the Claims**

The Examiner objected to the claims as being improperly numbered. In response, Applicant has appropriately amended claims 1-22. Accordingly, Applicant respectfully requests withdrawal of the objections to the claims.

**III. Disposition of the Claims**

Claims 1-22 are pending in the instant application.

**IV. Rejections Under 35 § 102**

The Examiner rejected claims 1-22 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,323,559 (the '559 patent) issued to Chan et al. Because of the reasons set forth below, reconsideration of the rejection is respectfully requested.

Independent claims 1, 6, 11, and 17 of the instant application require first and second bumps positioned on a first metal bar and a reference bump positioned on a second metal bar such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump is substantially equal to 150 degrees. Such an arrangement is exemplified in the embodiments shown in Figures 8a and 8b of the instant application.

The Examiner cited Figure 10 and related portions of the '559 patent as anticipating independent claims 1, 6, 11, and 17 and the remaining claims of the instant application. Figure

10 shows an arrangement in which alternating ground (VSS2) (280) and power (VDD2) (282) bumps are positioned. However, the '559 patent does not show or suggest that these bumps are disposed on metal bars as required by claims 1, 6, 11, and 17 of the instant application. In Figure 10, dotted encirclements shown around particular groups of bumps *do not* represent metal bars. Instead, the '559 patent refers to these bumps as being *internal logic* ground/power bumps. '559 patent, col. 7, lines 17-22. In the instant application, once a bump is fabricated, its connectivity to power or ground cannot be further designated because the bump is disposed on a metal bar that is either connected to Vdd or Vss. Specification, paragraph [0006]. Accordingly, the '559 patent fails to show or suggest bumps disposed on first and second metal bars as required by the claims of the instant application.

Moreover, the '559 patent is directed toward a bump arrangement in which bumps are hexagonally arranged. '559 patent, col. 3, lines 64-66. In Figure 10 of the '559 patent, bump groups are shaped as parallelograms. '559 patent, col. 7, lines 22-25. The Examiner stated that this arrangement anticipates the limitations of claims 1, 6, 11, and 17 of the instant application that require that a line from a reference bump to the first bump and a line from the reference bump to the second bump be substantially equal to 150 degrees. However, the first, second, and reference bumps to which the Examiner refers to here must be different from the first, second, and reference bumps referred to by the Examiner with respect to the first three elements of claims 1, 6, 11, and 17 because the bumps grouped in the parallelogram shape (290 in Figure 10 of the '559 patent) are wholly different from the bumps disposed on the purported first and second metal bars (280 and 282 in Figure 10 of the '559 patent). Assuming *arguendo* that the bumps grouped in the parallelogram shapes (290 in Figure 10 of the '559 patent) are disposed on alternating Vdd and Vss metal bars, there is no showing or suggestion, or statement/reasoning in the Office Action, as to how a 150 degrees angle is present with respect to these bumps. Referring to Figures 9 and 10 of the '559 patent, there is only a 60 degrees angle between a line from a reference bump (in a first row) to a first bump (in a second row) and a line from the reference bump to a second bump (in the second row). As described in the instant application, a realization of a close-to 150 degrees angle requires modification to the spacing between the bumps via modification to the spacing between metal bars. For example, as shown in Figures 8a and 8b of the instant application, the metal bars 52 and 54 are positionally brought in closer and

physically modified in order to achieve the 150 degrees angle recited in claims 1, 6, 11, and 17. The '559 patent wholly fails to show or suggest how a 150 degrees angle is or could be obtained. In other words, a mere grouping of bumps into parallelogram shapes in no way, mathematically or otherwise, shows or suggests how a 150 degrees angle is or could be achieved. Accordingly, the '559 patent fails to anticipate independent claims 1, 6, 11 and 17.

For the reasons set forth above, Applicant respectfully requests withdrawal of the rejection of independent claim 1, 6, 11, and 17. Claims 2-5, which depend from claim 1, claims 7-10, which depend from claim 6, claims 12-16, which depend from the claim 11, and claims 18-22, which depend from claim 17, are patentable for at least the same reasons.

**V. Conclusion**

The claims have been shown to be allowable over the prior art. Applicant believes that this paper is responsive to each and every ground of rejection cited by the Examiner in the Action dated August 14, 2002, and respectfully request favorable action in the form of a Notice of Allowance.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.147001/P6841).

Respectfully submitted,

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**APPENDIX A – SUBSTITUTE SPECIFICATION**



**APPENDIX B – MARKED-UP VERSION OF THE AMENDED CLAIMS**

[[c1]]1 An integrated circuit having a top metal layer, the top metal layer having a first metal bar and a second metal bar, the integrated circuit comprising:

- a first bump disposed on the first metal bar;
- a second bump disposed on the first metal bar; and
- a reference bump disposed on the second metal bar,

wherein the first bump and the second bump are positioned such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[[c2]]2 The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across the top metal layer to form a patterned bump array.

[[c3]]3 The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across a portion of the top metal layer.

[[c4]]4 The integrated circuit of claim 1, wherein the first metal bar is operatively connected to a voltage source, and wherein the second metal bar is operatively connected to ground.

[[c5]]5 The integrated circuit of claim 1, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

[[c6]]6 An integrated circuit having a top metal layer, the top metal layer having a first metal bar and a second metal bar, the integrated circuit comprising:

- a first bump disposed on the first metal bar;
- a second bump disposed on the first metal bar; and

a reference bump disposed on the second metal bar,  
wherein the first metal bar and the second metal bar are positioned such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[[c7]]7 The integrated circuit of claim 6, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across the top metal layer to form a patterned bump array.

[[c8]]8 The integrated circuit of claim 6, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across a portion of the top metal layer.

[[c9]]9 The integrated circuit of claim 6, wherein the first metal bar is operatively connected to a voltage source, and wherein the second metal bar is operatively connected to ground.

[[c10]]10 The integrated circuit of claim 6, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

[[c11]]11 A patterned bump array for a power grid of an integrated circuit, comprising:

a reference bump disposed on a first metal bar;

a first bump disposed on a second metal bar; and

a second bump disposed on a second metal bar,

wherein the first bump, the second bump, and the reference bump are arranged such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[[c12]]12 The patterned bump array of claim 11, wherein the first metal bar and second metal bar form a portion of the power grid.

[[c13]]13 The patterned bump array of claim 11, wherein the first metal bar is operatively connected to power, and wherein the second metal bar is operatively connected to ground.

[[c14]]14 The patterned bump array of claim 11, wherein the arrangement of the first bump, the second bump, and the reference bump is repeated across the power grid.

[[c15]]15 The patterned bump array of claim 11, wherein the arrangement of the first bump, the second bump, and the reference bump is repeated across a portion of the power grid.

[[c16]]16 The patterned bump array of claim 11, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

[[c17]]17 A bump layout for a power grid of an integrated circuit, comprising:

- a reference bump disposed on a first metal bar;
- a first bump disposed on a second metal bar; and
- a second bump disposed on a second metal bar,

wherein the first metal bar and the second metal bar are arranged such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[[c18]]18 The bump layout of claim 17, wherein the first metal bar and second metal bar form a portion of the power grid.

[[c19]]19 The bump layout of claim 17, wherein the first metal bar is operatively connected to

power, and wherein the second metal bar is operatively connected to ground.

[[c20]]20 The bump layout of claim 17, wherein the arrangement of the first metal bar and the second metal bar is repeated across the power grid.

[[c21]]21 The bump layout of claim 17, wherein the arrangement of the first metal bar and the second metal bar is repeated across a portion of the power grid.

[[c22]]22 The bump layout of claim 17, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.